Notice of Allowability	Application No.	Applicant(s)	
	10/708,096	CHOU ET AL.	
	Examiner	Art Unit	
	Than Nguyen	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *2/9/04*.

2. ☒ The allowed claim(s) is/are *1-21*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 2/9/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Claims 1-21 are pending.

2. The IDS, filed 2/9/04, has been considered.

Allowable Subject Matter

3. Claims 1-21 are allowed.

4. The following is an examiner's statement of reasons for allowance:

5. As to claims 1-13, the prior art does not fully teach nor suggest the serial flash memory chip. More specifically, the prior art does not further teach a serial flash-memory chip including a serial-bus interface to a serial bus connected to pins of the serial flash-memory chip, for transmitting and receiving serial data over the serial bus, a serial engine, coupled to the serial-bus interface, for converting serial data from the serial bus to parallel data; wherein the internal controller programs data into the EEPROM cells through the data buffers in response to a program flash command in a write-request packet received over the serial bus, whereby the serial flash-memory chip has a serial-packet interface for commands, address, and data.

6. As to claims 14-17, the prior art does not teach the combinations of a flash-memory chip with a serial-packet interface further comprising: a serial-bus interface to an external serial bus that transfers serial packets that include a memory-read-request packet, a memory-write-request packet, a configuration-read-request packet, and an input message packet input to the flash-memory chip, and a completion packet and an output message packet output from the flash-memory chip, reading a status from a configuration register identified by a header in the configuration-read-request packet to generate a data payload for the completion packet; erasing a

block of memory in the flash memory means in response to an erase indicator in a header in the input message packet and generating the output message packet once erasing is completed, and resetting the flash-memory chip in response to a reset indicator in a header in the input message packet, whereby operations are performed by the flash-memory chip in response to commands in serial packets received over the external serial bus include generation of completion packets with the data payload read from the flash memory means.

7. As to claims 18-21, the prior art does not teach the combinations of the claimed Peripheral Component Interconnect (PCI) Express flash-memory chip further comprising: a serial interface to external pins of the PCI Express flash-memory chip that connect to an external serial bus, the serial interface having a physical layer; wherein the external serial bus is a PCI Express serial bus having differential data lines that carry data serially; a controller, connected between the serial interface and the command register and data buffers, the controller comprising: a data-link layer that encapsulates transaction-layer packets for transmission over the external serial bus after framing by the physical layer; a transaction layer that generates headers to attach to data payloads to generate the transaction-layer packets; read operation means, responsive to a memory-read-request packet received over the external serial bus having a header with the flash address, for sending a read command to the command register and sending the flash address to the address decoders, and transferring data read from the EEPROM cells from the data buffers to the transaction layer as a data payload, the transaction layer attaching the data payload to a header to generate a completion packet with the read data, the completion packet being sent over the external serial bus as a response to the memory-read-request packet; program operation means, responsive to a memory-write-request packet received

over the external serial bus having a header with the flash address, for sending a write command to the command register and sending the flash address to the address decoders, and transferring data write from a data payload of the memory-write-request packet to the data buffers for writing to the EEPROM cells; erase operation means, responsive to a message packet received over the external serial bus having a header with an erase indicator, for sending an erase command to the command register, and generating a message packet for transmission over the external serial bus once the EEPROM cells have been erased; and reset operation means, responsive to a message packet received over the external serial bus having a header with a reset indicator, for sending a reset command to the control logic to reset the control logic and to reset the controller, whereby operations indicated by commands in serial packets received over the external serial bus are executed and data is returned in data payloads of serial packets.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is 571-272-4198. The examiner can normally be reached on 8am-3pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Than Nguyen
Primary Examiner
Art Unit 2187